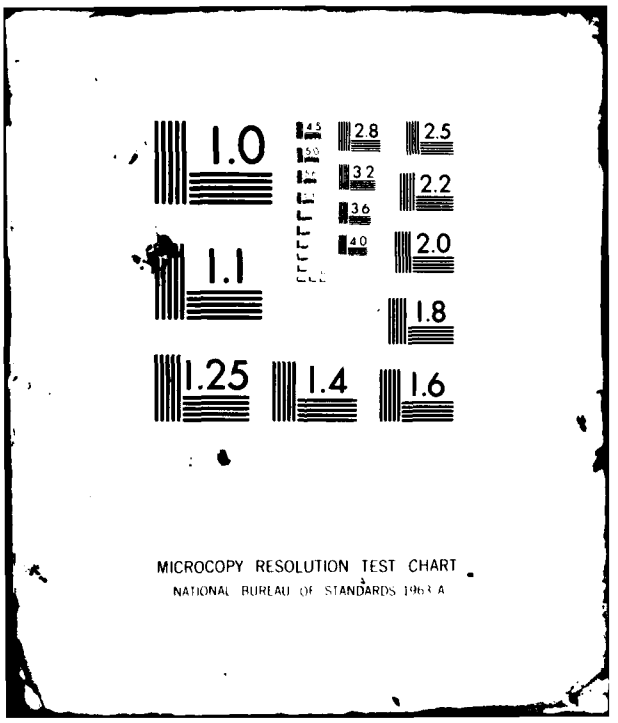
AD-A113 102 INSTITUTE FOR SOFTWARE ENGINEERING PALO ALTO CA F/G 9/2
AN/UYK-20 CAPACITY EXPERIMENT SPECIFICATION, NELC-UDI-A-106.(U)
JAN 78 L M TRAISTER N66001-77-C-0252
UNCLASSIFIED NL

END
DATE FILMED
5 82
DTIC


1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

PHOTOGRAPH THIS SHEET

AD A113102

DTIC ACCESSION NUMBER

II

LEVEL

I

INVENTORY

AN/UYK-20 Capacity Experiment Specification
NELC-UDI-A-106 Final Rept

DOCUMENT IDENTIFICATION

Contract N66001-77-C-0252 30 Jan. 78

DISTRIBUTION STATEMENT A
Approved for public release;
Distribution Unlimited

DISTRIBUTION STATEMENT

ACCESSION FOR	
NTIS	GRA&I
DTIC	TAB
UNANNOUNCED	
JUSTIFICATION	
BY	Per Ltr. on file
DISTRIBUTION /	
AVAILABILITY CODES	
DIST	AVAIL AND/OR SPECIAL
A-1	

DISTRIBUTION STAMP

DTIC COPY INSPECTED

DTIC
ELECTE
S APR 6 1982 D
D

DATE ACCESSIONED

DATE RECEIVED IN DTIC

PHOTOGRAPH THIS SHEET AND RETURN TO DTIC-DDA-2

DTIC FORM OCT 79 70A

DOCUMENT PROCESSING SHEET

AN/UYK-20 CAPACITY EXPERIMENT SPECIFICATION

NELC-UDI-A-106

FINAL REPORT

Prepared for:

NAVAL OCEAN SYSTEMS CENTER

Contract No. N66001-77-C-0252BW

Date: January 30, 1978

Prepared By: Leon M. Traister

INSTITUTE FOR SOFTWARE ENGINEERING

P.O. Box 637, Palo Alto, CA 94303

File 375-016

AN/UYK-20 CAPACITY

EXPERIMENT SPECIFICATION

NELC-UDI-A-106

FINAL REPORT

Prepared for:

NAVAL OCEAN SYSTEMS CENTER

Contract No. N66001-77-C-0252BW

Date: January 30, 1978

Prepared By: Leon M. Traister

INSTITUTE FOR SOFTWARE ENGINEERING

P.O. Box 637, Palo Alto, CA 94303

CONTENTS

SECTION 1
INTRODUCTION

1.0 GENERAL

This is the final report for the capacity experiment specification activity performed for the Naval Ocean Systems Center, San Diego, under Contract N6601-77-C-0252BW. This is a companion effort to the configuration capacity study for which the final report is concurrently submitted. Included in this report is an overview of verification objectives and methodology and a description of verification experiment conditions and parameters for specific AN/UYK-20 devices and configurations.

1.1 OBJECTIVES AND GOALS

This report will specify the experiments to be performed in order to verify the theoretically derived capacity (power) characteristics for the AN/UYK-20 CP and peripherals. These experiments create various of the conditions described by the capacity curves and equations for selected AN/UYK-20 configurations and will provide measured capacity data for comparison to predicted values.

Specifically, the experiments will:

i) Verify AN/UYK-20 device and configuration power equations and curves.

By using synthetic driver software to obtain sufficient calibration points, the conformance of measured data to that theoretically derived will be tested by examination of:

a) Function contour verification, i.e. functional conformance.
b) Accuracy of values - parameterization.
c) Actual ranges of proper device system interaction and function.

ii) Measure concurrent device and configuration power levels in several samples of field software, insofar as these are available. This process of "sizing" will establish instances of operating ranges derived from actual systems and applications software.

The following sections present first an outline of the components of the experiment design, to be completed in the anticipated experiment design phase of this contract for each of the experiments specified for AN/UYK-20 devices and configurations of the subsequent Section 3.

The experiment descriptions of Section 3 are thus intended to be input to the experiment design phase. The experiment parameters given are meant for guideline purposes, not strict adherence in the design process. Actual values selected may vary depending on equipment availability, convenience of setup and the like.

Not mentioned in the experiment specifications are the specific component quantities to be measured for the derivation of power values. These too are to be fully developed in the experimental design phase. The specifications are to give the substance of the experiments required to verify the power equations.

Frequent reference will be made to the companion report under this contract, the "AN/UYK-20 CAPACITY CALCULATIONS, FINAL REPORT." For brevity, we will refer to it simply as the "Capacity Calculations Report."

SECTION 2

METHODOLOGY

2.0 GENERAL

This section provides an outline of the components of the verification experiment designs which are themselves specified in the next section. It is the anticipated experiment design phase of this contract which will provide the performance details for what is described in these two sections.

2.1 CONTENT OF EXPERIMENT DESIGNS

(a) Purpose of Experiment - the power/capacity measurement sought for verification and the configuration context and workload.

(b) The strategy of verification

  (1) background theory
  (2) directly measured and derived quantities
  (3) broad measurement technique

(c) Software driver requirements (calibration)

(d) Hardware and configuration requirements

(e) Environmental considerations (if pertinent)

(f) Auxiliary data requirements - prerecorded tape or disk (if pertinent)

(g) Measurement specifics (calibration or field software sizing)

  (1) instrumentation
  (2) probe points
  (3) parameters and conditions
  (4) the experiment scenario, recorded data

(h) Data reduction

  (1) deriving the experimental power data and curves
  (2) error analysis, accuracy of results

(i) Evaluation

(1) calibration - methodology for determining functional fit and accuracy

(2) field software sizing methodology.

SECTION 3

EXPERIMENT SPECIFICATIONS

3.0 GENERAL

This section provides basic descriptions of the experiments required for the verification of the power (capacity) equations and curves of the Capacity Calculations Report. Parameters given in this description are generally intended as guidelines for the verification. Fixing of these values and conditions is appropriate to the experiment design and performance phases of this contract.

3.1 THE EXPERIMENT ENVIRONMENT

It is expected that all experiments will be performed under laboratory conditions with ambient temperature at 25°C nominal and with supply voltages within the manufacturer's specified tolerances.

Ambient temperatures substantially different from 25°C will cause a slowdown of the AN/UYK-20 master clock and a lengthening of the storage cycle time. For this reason, it may be necessary to recompute certain of the theoretical power values for the CP using actual master clock and memory cycle times, as measured at the time of the verifying experiments, in order to assure a valid basis for comparison.

3.2 DEVICES AND CONFIGURATIONS

3.2.1 AN/USH-26 CMTU POWER

3.2.1.1 The AN/USH-26 cartridge magnetic tape unit is described in Sections 2.1 and 2.2 of the Capacity Calculations Report. The specified experiments will verify the validity of the theoretical state charts and the drive, configuration and channel power equations and values.

3.2.1.2 Drive/Controller/Channel Configuration Powers

i) State chart verification (Capacity Calculations Report Figure 2.2) Device, controller and channel busy state verification during:

a) Read
b) Write
c) Space File
d) Space Block
e) Write Tape Mark
f) Erase

ii) Read/Write Power (Capacity Calculations Sec. 2.4)
Verify Capacity Calculations Report Equation 2.1 at blocksizes: 80, 120, 250, 500, 1000, 2000, 4000, 10,000, 20,000, 40,000.

3.2.2 AN/USH-23 (Model 3500) DISK SYSTEM POWER

3.2.2.1 The AN/USH-23 (System Industries Model 3500) disk system with Diablo Series 30 drives is described in the Capacity Calculations Report Section 3.1.

3.2.2.2 Series 30 Drive Power - 12 sector/track format

i) Drive State Chart Verification (Capacity Calculations Report Figure 3.1)
Verify device busy states during read/write while sectors, tracks and cylinders are spanned in one I/O operation.

ii) Read/Write power - calibration (Capacity Calculations Report Section 2.3.2)
Verify the Capacity Calculations Report Equation 3.5 for read/write using blocksizes:

a) 1, 256, 512, 513, 768, ..., 5120 Bytes; 5633, 5880, 6144, 6145 (track boundary), 6400, 6656 Bytes
b) 11777, 120320, 12288, 12289 (cylinder boundary), 12544, 12800 Bytes
c) 3 cyls, 3 cyls ± 1, ± 256, ± 512 Bytes
d) 5 cyls, 5 cyls ± 1, ± 256, ± 512 Bytes

e) 10 cyls, 10 cyls ± 1, ± 256, ± 512 Bytes

f) 20 cyls, 20 cyls ± 1, ± 256, ± 512 Bytes

g) 50 cyls, 50 cyls ± 1, ± 256, ± 512 Bytes

h) 100 cyls, 100 cyls ± 1, ± 256, ± 512 Bytes

i) 200 cyls, 200 cyls - 1, -256, -512, Bytes (full pack)

for initial seeks equivalent to 0, 70, 100 msec.

3.2.2.3 AN/USH-23 (Model 3500) Control Unit/Channel Power

i) State Chart Verification (Capacity Calculations Report Section 3.3.1).

a) Verify the Control Unit and channel busy states of the Capacity Calculations Report Figure 3.2 while sectors, tracks and cylinders are spanned in one I/O operation on a single Series 30 drive.

b) Determine with 2 through 8 Series 30 drives split over 2 controllers and on a single channel, the percent time for which the conditions of the Capacity Calculations Report state chart of Figure 3.3 can be established when $t_{10} \leq (N-1)t_{\phi}$ as described in that report's Section 3.3.2.1. This verification is to be performed for seek times: $t_{10} = 0$ and one non-zero value with logical record lengths of 1024, 2048, 8192 and 16384 bytes.

c) Determine with 2 through 8 Series 30 drives split over 2 controllers and a single channel, the precent time for which the conditions of the Capacity Calculations Report state chart of Figure 3.4 can be established when $t_{10} \geq (N-1)t_{\phi}$ as described in that report's Section 3.3.2.2. This verification is to be performed for seek times 70 and 130 msec and as many of the logical record lengths of b) as possible such that $t_{10} \geq (N-1)t_{\phi}$.

d) Power Value Verification

For the conditions of item i), above, determine by measurement the validity of the Case 1 and Case 2 Power Equations (3.6) and (3.7) in the Capacity Calculations Report.

3.2.3 AN/USQ-69 (ADD) Display Power

3.2.3.1 The AN/USQ-69 Alphanumeric Digital Data (ADD) Display is described in Section 4.2 of the Capacity Calculations Report. The specified experiments will verify the validity of the block output mode theoretical state chart and the single display/channel output power for certain of the MIL-STD-1397 and MIL-STD-188 channel/interfaces.

3.2.3.2 ADD Display Power

i) Device State Chart Verification (Capacity Calculations Report Section 4.3.3)

The validity of the state chart of Figure 4.1 in the Capacity Calculations Report is to be tested, that is, the channel, control unit and display busy states are to be verified for the periods shown in the diagram. This is to be done for one parallel and one serial interface.

ii) Output Power - calibration (Capacity Calculations Report Section 4.3.3)

It will be sufficient to verify the Capacity Calculations Report power equation (4.1) for one of the parallel interfaces as the state chart validity for both serial and parallel interfaces implies a predictable data transmit and memory write time for any interface and a fixed settling scan time. Hence, if the validity of the state chart is shown as per i), above, ADD output power becomes a function of interface/channel speed.

3.2.4 CHANNEL DEVICE AND CONFIGURATION POWERS

3.2.4.1 The parallel and serial I/O channels for the AN/UYK-20 are described in Sections 5.2.1 and 5.2.2 of the Capacity Calculations Report. The specified experiments will verify the nominal power limits for parallel channel groups and for the total AN/UYK-20 IOC/channel configuration.

3.2.4.2 Parallel Channel Groups - calibration (Capacity Calculations Report Section 5.2.1)

i) Verify the maximum input, output and concurrent input/output powers for a single channel group for the MIL-STD-1397 types A and B or C channels in single (16 bit) mode as shown in the Capacity Calculations Report Table 5.1. Verification will consist of determining the peak powers for these conditions and interfaces and comparing these with the theoretical values.

ii) Similarly verify the operation of MIL-STD-1397 types A and B or C channels in dual (32 bit) mode using a pair of channels $n,n+4$ each in a separate channel group.

3.2.4.2 Channel Configuration Power (calibration and sizing) (Capacity Calculations Report Section 5.3.1)

i) Verify the 2000 KW/S nominal limit for IOC input/output power.

ii) Size applications and systems software units to determine peak and average IOC and channel configuration powers used.

3.2.5 AN/UYK-20 CP POWER

3.2.5.1 Basic AN/UYK-20 CP architecture and characteristics are described in Section 6.2 of the Capacity Calculations Report. The models for interaction of the IOC and the DMA facility with the CP are described in Sections 6.4.2 and 6.5.2, respectively of the same report.

The specified calibration experiments will verify the CP instruction powers of several individual AN/UYK-20 repertoire instructions. The power of the restricted instruction mixes and that of the general SPERRY-UNIVAC PX 11901 instruction mix, each described in Section 6.4.5 of the Capacity Calculations Report, will be determined. Finally, the interactive effects of concurrent IOC or DMA facility power on the CP as developed in the Capacity Calculations Report Sections 6.4.4 - 6.4.5 and 6.5.3 - 6.5.4 will

be tested on selected instructions and mixes. Additionally, a sizing experiment is proposed using field software to determine actual levels of CP powers used and of CP-IOC and CP-DMA interaction.

3.2.5.2 Instruction Power Verification

i) Calibration

The absolute instruction powers of the following instructions are to be determined both individually and as workload power in a mix consisting of the following instructions (the SPERRY-UNIVAC PX-11901 General Mix):

a)	22 RI Add	17%
b)	22 RX Add	17%
c)	31 RI Logical	17%
d)	31 RX Logical	17%
e)	44 RI Jump	12%
f)	44 RX Jump	6%
g)	26 RX Multiply	4%
h)	26 RI Multiply	1%
i)	27 RK Divide	1%
j)	Miscellaneous	8%

The measured powers are to be compared to the theoretical powers computed using the published instruction timings in the AN/UYK-20 Technical Description Manual, SPERRY-UNIVAC #PX-10431C, according to the methods of the Capacity Calculations Report Section 6.3.2. The measured average workload CP power is to be compared with the proportional sums of the individual measured powers, thus validating Equation (6.5) of the Report.

ii) Field Software Sizing

The average workload CP power of several field software units is to be measured. These powers are to be determined both as absolute (T_x = execution time of the CP) and as relative to the Γ-processor (T_x = execution time of the Microprogrammed Controller).

3.2.5.3 IOC Activity-Degraded CP Power (calibration)

The CP Execution Time and Power Factors $\eta(\phi)$ and $\xi(\phi)$ defined by Equation (6.8) in the Capacity Calculations Report are to be determined for the individual instructions a) through i) in Section 3.2.5.2, above, and for the mix of these constituent instructions in the specified percentages.

Sufficiently many levels of IOC input, output, 16-bit and 32-bit power are to be established so as to verify the Capacity Calculations Report Equation Series (6.10) through (6.13). Note that the Equation Series (6.13) is for the General Mix and so it and the curves of the Figure 6.4 (and hence of Figure 6.5) in the Capacity Calculations Report are to be verified using values of ξ computed for measured <u>average</u> levels of relative CP power.

The Equation (6.14) of the Capacity Calculations Report is to be verified formally by comparing measured <u>average</u> levels of relative CP power for the PX-11901 General mix to values obtained by substituting in the equation values of $\eta(\phi)$, the reciprocals of the <u>measured</u> values of $\xi(\phi)$, and the values of <u>measured</u> individual absolute instruction powers.

3.2.5.4 DMA Activity-Degraded CP Power (calibration)

i) DMA-Installed Instruction Times and Powers

As the presence of the DMA facility affects instruction timing and hence power, it will be necessary to verify the published times in the SPERRY-UNIVAC publication #PX-11772 for the instructions in the PX-11901 General Mix (described in Section 3.2.5.2, above). The experiments of Section 3.2.5.2, above, are to be repeated for an AN/UYK-20 with the DMA installed, and the power values obtained are to be compared to those computed according to the methods of the Capacity Calculations Report Section 6.3.2 using instruction times from the PX-11772 publication.

ii) Verification of $\mu(\phi_D)$ and $\xi(\phi_D)$

The common memory bank DMA Power-Degraded Instruction Time Augmentation Factor, $\mu(\phi_D)$, derived from Equation (6.15) of the Capacity Calculations Report is to be verified for the individual instructions of the PX-11901 General Mix. An average value of the $\mu(\phi_D)$ is to be determined for the mix as a whole by measurement.

The Equation (6.18) in the Report is to be formally verified by comparing measured average levels of selective CP Power for the PX-11901 General Mix to values obtained by substituting in the equation values of $\mu(\phi_D)$ and individual absolute instruction powers derived by measurement.

Finally, the DMA-Degraded Instruction Execution Power Factor, $\xi(\phi_D)$, is to be experimentally determined from measurements of relative CP power for the individual constituent instructions of the General Mix and from measurements of average relative CP Power for the General Mix as a whole. This will verify the Table 6.5 and Figure 6.7 in the Capacity Calculations Report for the 22 RI Add and 22 RX Add instructions as well as the methodology of Section 6.5.4 of the Report.